Novel Photo-Defined Polymer-Enhanced Through-Silicon Vias for Silicon Interposers

Paragkumar A. Thadesar, *Student Member, IEEE*, and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*— This paper presents a silicon interposer interconnection solution featuring novel electrical and optical through-silicon vias (TSVs). The copper-based electrical TSVs include polymer-clad TSVs and polymer-embedded vias (copper vias embedded in polymer wells within a low resistivity silicon substrate). Fabrication of the novel electrical TSVs is shown along with high-frequency measurements for polymer-embedded vias. Optical TSVs are fabricated in parallel with the polymer-clad TSVs to provide chip-to-motherboard optical access at the 850-nm wavelength. Optical loss measurements are performed for the fabricated optical TSVs.**

***Index Terms*— Electrical loss measurements, electrical resistance measurements, lithography, optical interconnections, optical loss measurements, through-silicon vias (TSVs).**

I. Introduction

IN MODERN computing systems, the demand for high bandwidth communication between chips (required to improve the system throughput) has exacerbated with the transition to multicore processors [1]–[3]. Therefore, chip-to-chip interconnection has emerged as a key performance limiter to system performance. To mitigate this issue, the use of a silicon interposer with through-silicon vias (TSVs) is widely explored as it enables multiple chips to be interconnected using a denser lateral metallization relative to organic or ceramic substrates [4]–[7]. This results in high bandwidth-density communication between the chips [8]. For longer interconnect distances that traverse the motherboard (between chips on different silicon interposers, for example), optical interconnects may provide a path for higher bandwidth and lower energy communication relative to conventional electrical interconnects [9]. As such, there is a need to integrate optical links with conventional electrical interconnects, including at the silicon interposer level [10].

Increasing the silicon thickness minimizes warpage of a large area interposer [11]. However, it increases TSV length, leading to an increase in TSV capacitance and RF losses [12], [13]. Additionally, the TSV RF losses are higher in low resistivity silicon that has lower cost relative to high resistivity silicon [14], [15]. In addition, the coefficient of thermal expansion (CTE) mismatch between copper and silicon can result in high TSV stresses [16]. To address these challenges as well as to integrate optical links for a high speed and high bandwidth interposer-to-interposer communication, we propose a thick silicon interposer interconnection solution featuring novel polymer-enhanced photo-defined electrical and optical TSVs (Fig. 1). The two novel electrical TSVs presented in this paper are polymer-clad TSVs and polymer-embedded vias.

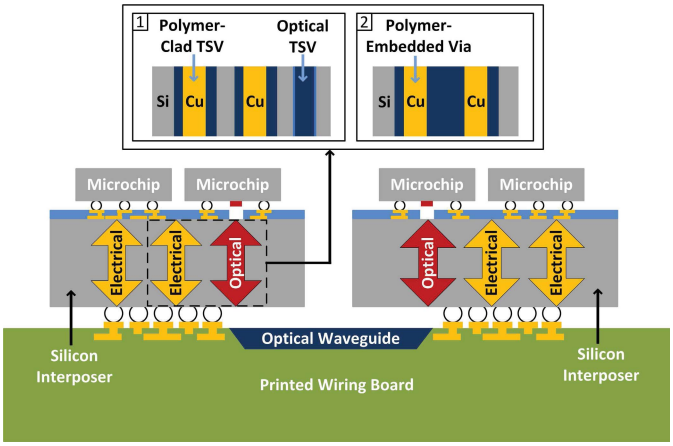

Fig. 1. Silicon interposers featuring our novel polymer-enhanced electrical and optical TSVs. 1: Polymer-clad TSVs and optical TSVs that can be fabricated simultaneously. 2: Polymer-embedded vias.

Polymer-clad TSVs consist of a photo-defined thick ($\sim$20 μm) polymeric cladding (liner) instead of a conventional thin ($\sim$1 μm) silicon dioxide liner between the copper vias and silicon. A reduction in TSV dielectric capacitance and TSV loss can be obtained using a thick cladding [17]–[19]. In addition, a thick polymeric cladding with a Young's modulus lower than copper and silicon can absorb stresses caused by the CTE mismatch between the copper and silicon, thereby relieving TSV stresses [20], [21]. The proposed polymer-clad TSVs in this paper can be fabricated simultaneously with polymer-based optical TSVs, providing a low-cost and wafer-level batch fabrication platform for electrical and optical TSVs in silicon interposers. Additionally, to obtain even further reduction in TSV RF losses compared with the polymer-clad TSVs, novel photo-defined polymer-embedded vias are reported, as shown in Fig. 1. Polymer-embedded vias consist of copper vias embedded in photo-defined polymer wells within low resistivity silicon. Therefore, polymer-embedded vias possess the cost advantage of low resistivity silicon.

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The authors are with the Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: pthadesar3@gatech.edu; muhannad.bakir@mirc.gatech.edu).

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TABLE I
COMPARISON OF TSV POLYMER CLADDING FABRICATION PROCESSES

	Fabrication Method	Principle	Benefit	Limitation
1	**Vapor deposition [24]**	Deposition of parylene	Deposition at room temperature	Limited cladding thickness
2	**Circular trench polymer filling [25]**	Polymer filling in etched circular trench followed by removal of silicon from center	Flexibility in polymer material selection	High aspect-ratio polymer filling may be difficult
3	**Laser ablation [26]**	Serial ablation of polymer filled in vias	Panel-scale fabrication possible	Serial process and precision of ablation
4	**Photo-definition with a release film (for coaxial TSVs) [23]**	Photo-definition of polymer-filled vias with a temporary release film at the base	Knowledge of high aspect-ratio photo-definition easily available in literature	Temporary release film needed to support polymer and limited selection of high aspect-ratio photo-definable materials
5	**Photo-definition with mesh (The concept presented in this paper)**	Photo-definition of polymer-filled vias with a mesh layer at the base	Knowledge of high aspect-ratio photo-definition easily available in literature and mesh helps for void-free polymer filling and bottom-up electroplating	Limited selection of high aspect-ratio photo-definable materials

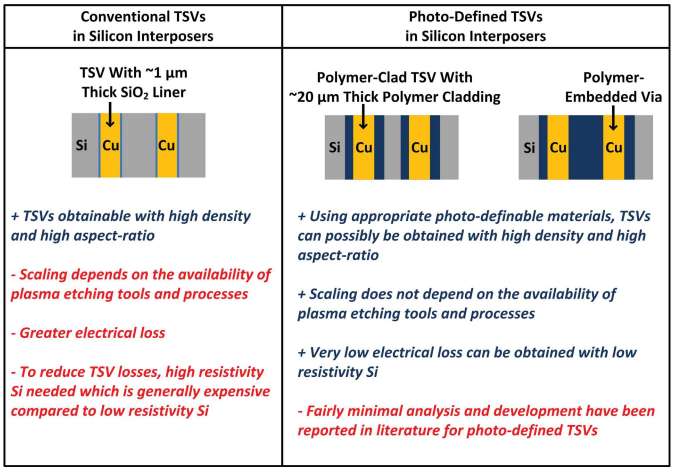


Fig. 2. Comparison between conventional and photo-defined TSVs for silicon interposers.

The fabrication of the proposed TSVs in this paper differs from the fabrication of conventional TSVs principally because of the fact that the fabrication of the proposed TSVs leverages the advantage of high aspect-ratio dielectric photo-definition [22], as shown in Fig. 2. In conventional TSV fabrication, the diameter and aspect-ratio scaling depend on the availability of plasma etching tools and processes. Whereas for the proposed TSVs obtained using dielectric photo-definition, etching requirements are relaxed as a larger area (via or trench) can easily be etched in silicon followed by polymer filling, photo-definition, and electroplating. There is fairly minimal analysis and technological development reported in literature for photo-defined TSVs; S. W. Ho *et al.* [23] have shown the fabrication of coaxial TSVs using photo-definition to obtain impedance matching.

Hence, the rationale behind this research is to investigate and advance the fabrication process of photo-defined TSVs that provide lower loss compared with conventional TSVs. This paper describes the fabrication of the novel TSVs under consideration in Section II. Section III reports electrical and optical measurements of the novel electrical and optical TSVs, respectively.

II. FABRICATION PROCESSES AND RESULTS

A. Photo-Defined Polymer-Clad and Optical TSVs

This section focuses on the fabrication of photo-defined polymer-clad TSVs and optical TSVs, which can be formed simultaneously. Prior efforts in the fabrication of polymer cladding for TSVs have utilized polymer vapor deposition [24], polymer filling in circular trenches [25], laser ablation of polymer-filled vias [26], and photo-definition of polymer-filled vias with a temporary release film to obtain coaxial TSVs [23]. This paper reports a novel photo-definition process with a mesh layer to obtain high aspect-ratio polymer-clad TSVs. To better differentiate the polymer cladding fabrication processes, a comparison is shown in Table I.

To fabricate the polymer cladding, SU-8 [22] is used in this paper as it can provide high aspect-ratio photo-defined structures with relative ease compared with other photo-definable materials. Research on the investigation of different photo-definable materials, in addition to SU-8, is in progress. Thick SU-8 cladding can provide a reduction in TSV losses as well as a possible reduction in TSV stresses as the Young's modulus of SU-8 (4.02 GPa) is lower relative to that of copper and silicon [22].

As shown in Fig. 3, the fabrication process for polymer-clad TSVs begins with the deposition of silicon dioxide on the back side of a silicon wafer. Next, using the Bosch process [27], vias are etched in the silicon; a negative photoresist (Futurrex) mask is used during the Bosch process. Once the vias are etched, a pattern of microvias (called mesh [28]) is formed in the silicon dioxide suspended membrane at the base of the vias. Next, SU-8 is spin coated to fill the vias. Following a soft bake, the SU-8-filled vias are optically defined using UV exposure followed by a post exposure bake and SU-8 development to yield SU-8-clad vias. The optical definition is performed with exposure from the mesh end of the vias as it is smoother compared with the nonmesh end of the vias. Once

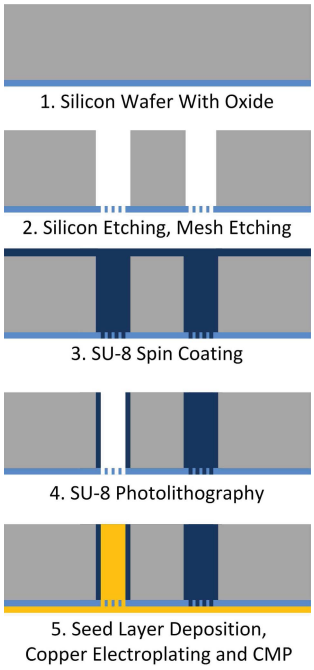
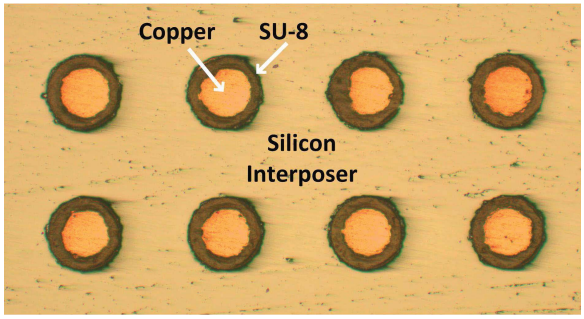


Fig. 3. Fabrication process for simultaneous fabrication of photo-defined polymer-clad and optical TSVs.



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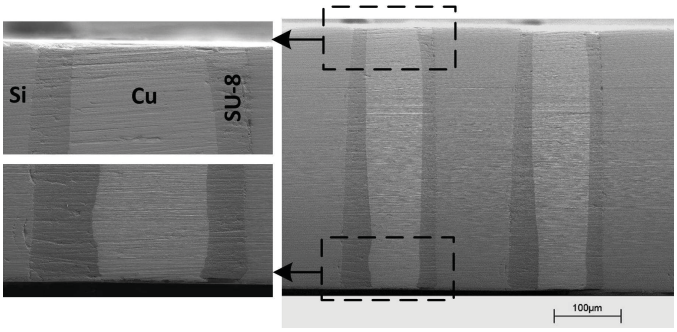

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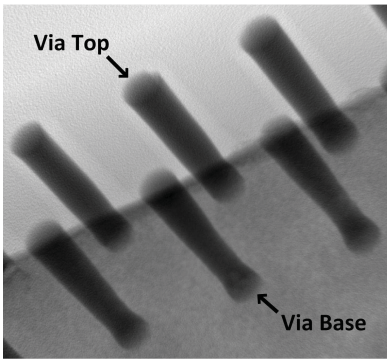


(c)

Fig. 4. Fabricated 390-μm tall SU-8-clad TSVs with ~80-μm diameter copper vias surrounded by a ~20-μm thick cladding on a 250-μm pitch. (a) Top view. (b) Cross-section view. (c) X-ray image showing void-free copper electroplating.

the SU-8 cladding is fabricated, a titanium-copper seed layer is deposited on the mesh side. The titanium layer is used to obtain adhesion between the copper and the silicon dioxide. After seed layer deposition, electroplating is performed over the mesh side to pinch off the openings in the mesh followed by bottom-up copper electroplating and chemical mechanical polishing (CMP) to remove overburden copper.

As shown in Fig. 4(a) and (b), 390-μm tall copper TSVs with ~80-μm diameter and surrounded by a ~20-μm thick SU-8 cladding are fabricated on a 250-μm pitch. Void-free copper electroplating is obtained, as shown in the X-ray image [Fig. 4(c)] of the fabricated polymer-clad TSVs.

Deposition of barrier and adhesion layers is commonly demonstrated in literature for the conventional TSVs fabricated using superfill electroplating [29] and can be adopted in the proposed polymer-clad TSVs.

Fig. 5 shows the distribution of the fabricated copper via diameters obtained using the described photo-definition process. The average measured copper via diameter at the top (nonmesh) end is 81 μm with a standard deviation of 8.3 μm, and the average measured copper via diameter at the mesh end is 63.5 μm with a standard deviation of 3.4 μm. Further process optimization would address this issue.

In addition, as shown in Fig. 3, optical TSVs can be obtained simultaneously with polymer-clad TSVs using the same photo-definable polymer (SU-8). As SU-8 has good optical transmission characteristics in the window of 850-nm wavelength, and optical interconnects have been demonstrated using SU-8 [30], it is selected as the core of the optical TSVs; silicon dioxide is used as the cladding to obtain total internal reflection.

With respect to the fabrication of optical TSVs, the etched vias in silicon are filled with SU-8, followed by SU-8 soft bake similar to the fabrication of polymer-clad TSVs. However, during the UV exposure step for the polymer-clad TSVs, the polymer-filled vias intended for optical TSVs are simply flood exposed. As SU-8 is negative tone, the polymer remains in the flood-exposed vias at the end of the SU-8 development, yielding the optical TSVs.

As shown in Fig. 6, 390-μm tall optical TSVs are fabricated with a 118-μm diameter SU-8 core surrounded by a 2-μm thick silicon dioxide cladding.

B. Polymer-Embedded Vias

In addition to polymer-clad and optical TSVs, polymer-embedded vias are also fabricated using SU-8. As shown in Fig. 7, the fabrication of polymer-embedded vias begins with the deposition of silicon dioxide, titanium (for adhesion between silicon dioxide and copper), and copper on one side of a silicon wafer. Next, using the Bosch process [27], wells

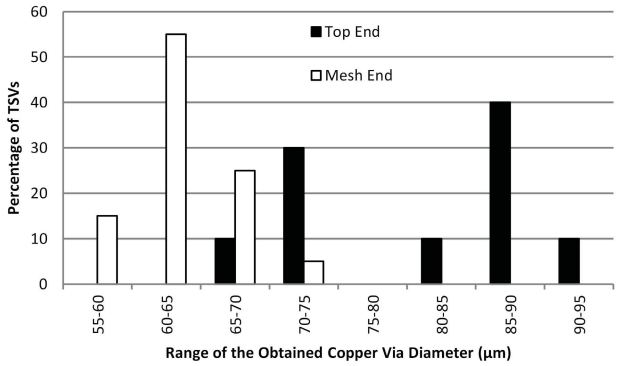


Fig. 5. Distribution of the obtained copper via diameters of 20 measured polymer-clad TSVs.

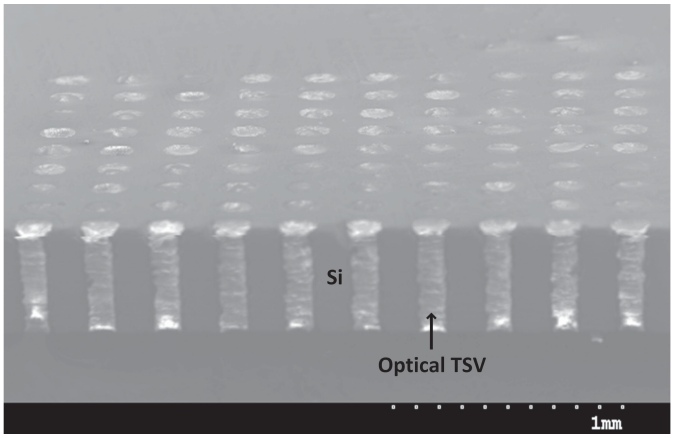


Fig. 6. Fabricated 390-μm tall optical TSVs with a 118-μm diameter SU-8 core surrounded by a 2-μm thick silicon dioxide cladding on a 250-μm pitch.

are etched in the silicon wafer using a photoresist mask. After silicon etching, the silicon dioxide and the titanium layers are etched using buffered oxide etch. Next, SU-8 is spin coated on the wafer to fill the trenches followed by a soft bake and UV exposure of the vias in the SU-8-filled wells [31]. Once a post exposure bake is completed, SU-8 development is performed yielding vias in the SU-8-filled wells, as shown in Fig. 8. The fabricated vias are observed to have tapered sidewalls, resulting in greater diameter at the base of the vias. Further research on optimization of the fabrication process to minimize the taper is in progress. Following via development, bottom-up copper electroplating of the vias is performed, followed by CMP to remove overburden copper.

Fig. 9(a) is a top-view image of the fabricated 270-μm tall and 100-μm diameter polymer-embedded vias on a 250-μm pitch. Fig. 9(b) is a cross-section image illustrating the polymer-embedded vias; the approximate taper for each of the shown vias is also shown for completeness.

In addition, we demonstrate the scaling of the polymer-embedded vias by fabricating 65-μm diameter and 270-μm tall polymer-embedded vias on a 250-μm pitch, as shown in Fig. 9(c). Similar to polymer-clad TSVs, void-free copper electroplating is obtained for the fabricated polymer-embedded vias, as shown in the X-ray image [Fig. 9(d)]. In addition, superfill electroplating process with the deposited barrier and

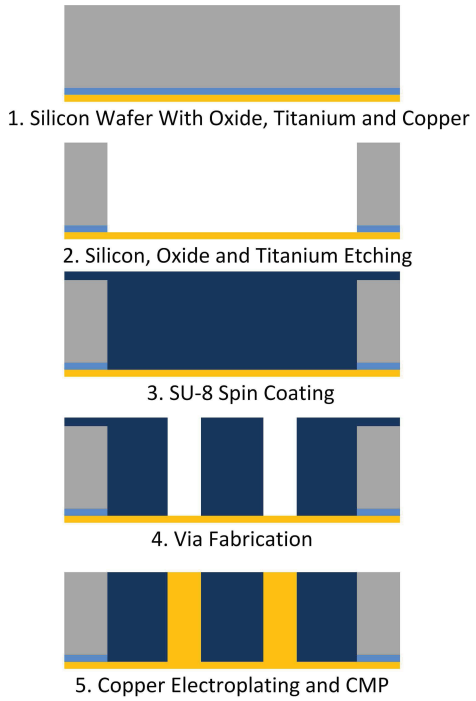


Fig. 7. Fabrication process for polymer-embedded vias.

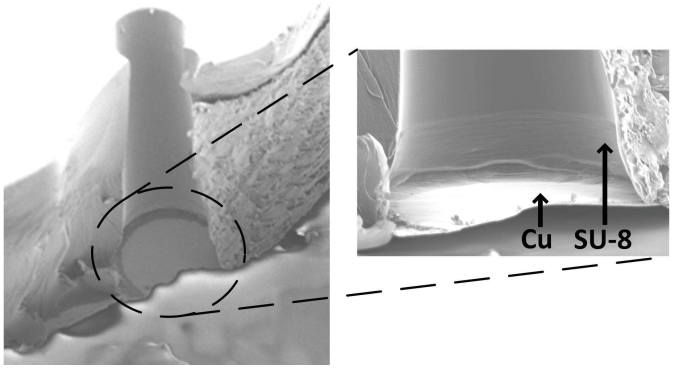


Fig. 8. Cross-section of a polymer-embedded via after SU-8 development and magnified image of via base, which shows diameter widening.

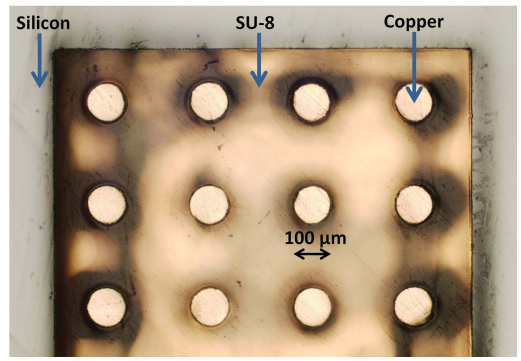
adhesion layers over the via side walls can be adopted in the future for the demonstrated polymer-embedded vias.

III. Characterization

A. High-Frequency Measurements of Scaled Polymer-Embedded Vias

As inset in Fig. 10(b), a TSV-trace-TSV structure is implemented for high-frequency measurements of the fabricated polymer-embedded vias. The metal traces connecting the TSVs are 190-μm wide and 1-μm thick. For the measurements, a dedicated RF probe station setup is used with Agilent N5245A PNA-X network analyzer and Cascade |Z| probes. LRRM calibration protocol is implemented prior to the TSV measurements to de-embed the measurements of the device under test.

Once the setup is calibrated, high-frequency measurements are performed from 100 MHz to 50 GHz for the fabricated



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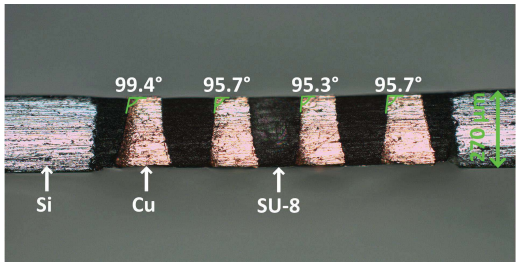

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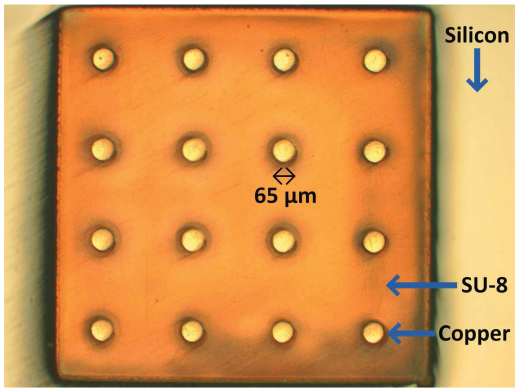

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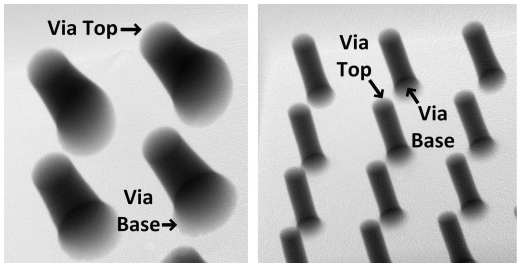
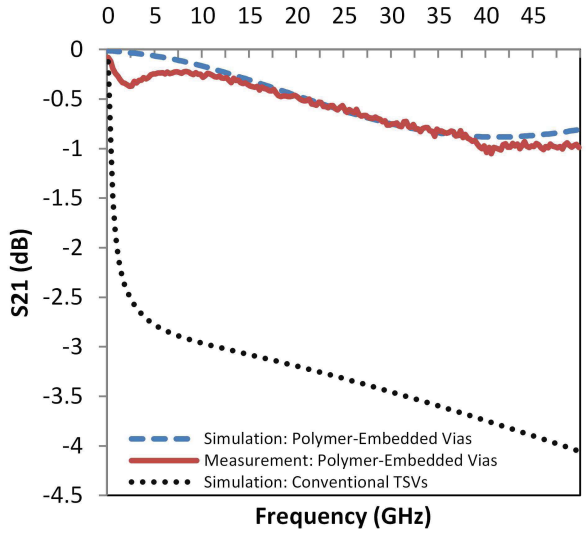


(d)

Fig. 9. Fabricated 270-μm tall polymer-embedded vias on a 250-μm pitch. (a) Top view of 100-μm diameter TSVs. (b) Cross-section view of 100-μm diameter TSVs. (c) Top view of 65-μm diameter TSVs. (d) X-ray image showing void-free copper electroplating of 100-μm diameter TSVs (left) and 65-μm diameter TSVs (right).



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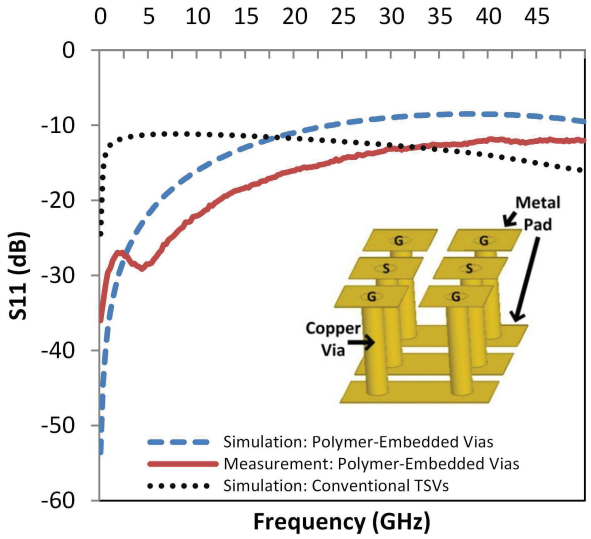


(b)

Fig. 10. High-frequency simulation and measurement results for the fabricated TSV-trace-TSV structure of 65-μm diameter polymer-embedded vias and simulations for conventional TSVs with 1-μm thick silicon dioxide liner and the same copper via dimensions. (a) Insertion loss measurements and simulations. (b) Reflection loss measurements and simulations. Inset: TSV-trace-TSV structure.

270-μm tall and 65-μm diameter polymer-embedded vias on a 250-μm pitch, as shown in Fig. 10. The measured insertion loss is approximately 1 dB at 50 GHz. To validate the measurements, full-wave electromagnetic simulations of polymer-embedded vias are performed in High Frequency Structure Simulator (HFSS) from 100 MHz to 50 GHz with 3.25 and 0.035 as the relative dielectric constant and the loss tangent of SU-8, respectively [23]. In addition, as shown in Fig. 10, to compare the high-frequency characteristics of the fabricated polymer-embedded vias to conventional TSVs, HFSS simulations are performed for conventional TSVs with 1-μm thin silicon dioxide liner and the same copper via dimensions. The relative dielectric constants of silicon and silicon dioxide are 11.68 and 3.9, respectively [32]. A reduction in TSV insertion loss is observed for the fabricated polymer-embedded vias compared with the conventional TSVs. This can be due to the lower material loss of the polymer compared with silicon as well as to the matching of the structure to 50 Ω characteristic impedance [33].

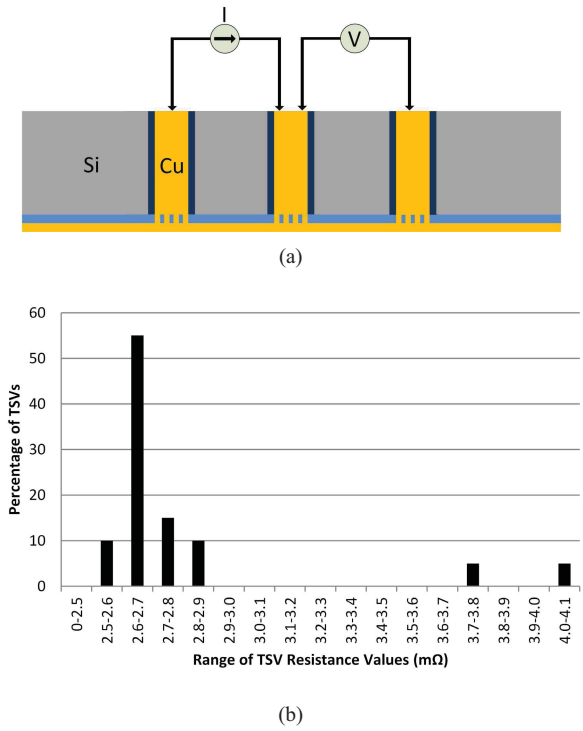


Fig. 11. Four-point resistance measurements for the fabricated polymer-clad TSVs. (a) Four-point resistance measurement setup. (b) Distribution of the measured resistance values.

B. Resistance Measurements

Four-point resistance measurements are performed for the fabricated polymer-clad TSVs and polymer-embedded vias, as shown in Figs. 11 and 12.

With respect to the polymer-clad TSVs, the average measured resistance of 20 different SU-8-clad TSVs with ~80-μm diameter copper vias, ~20-μm thick cladding, and 390-μm tall is 2.81 mΩ. Fig. 11(b) shows the distribution of the measured polymer-clad TSV resistances. With respect to the polymer-embedded vias, the average measured resistance of 20 different 270-μm tall polymer-embedded vias with 100-μm diameter is 2.54 mΩ and with 65-μm diameter is 2.77 mΩ. Fig. 12(b) and (c) show the distribution of the measured polymer-embedded via resistances.

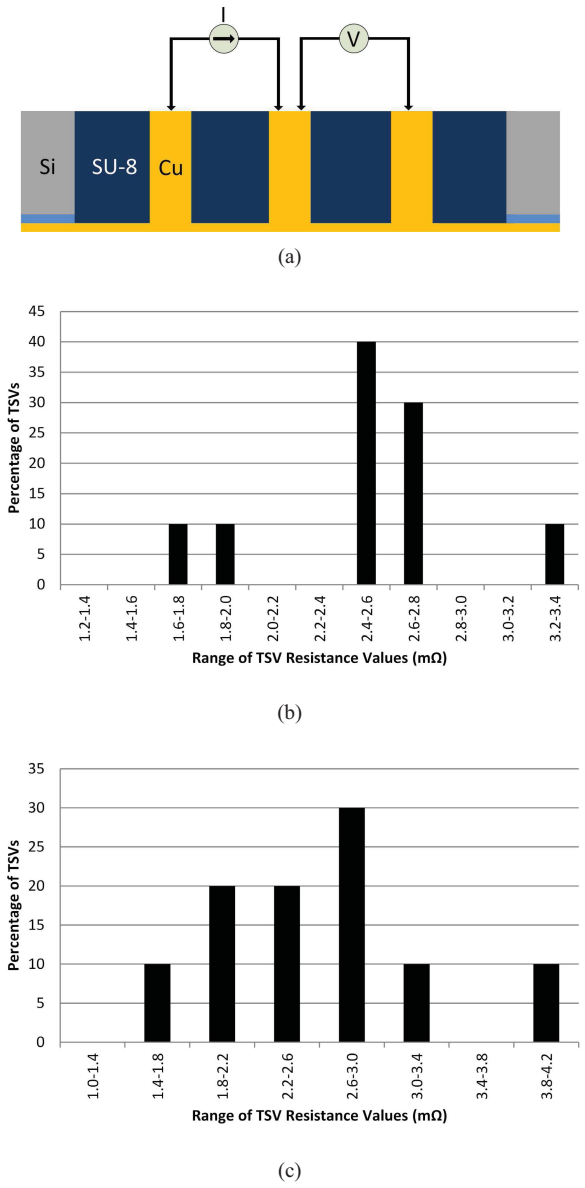


Fig. 12. Four-point resistance measurements for the fabricated polymer-embedded vias. (a) Four-point resistance measurement setup. (b) Distribution of the measured resistance values of 100-μm diameter vias. (c) Distribution of the measured resistance values of 65-μm diameter vias.

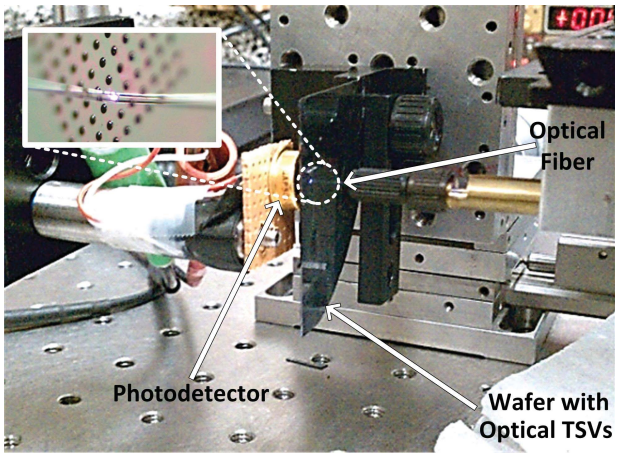
C. Optical Loss Measurements

As shown in Fig. 13(a), an experimental setup is established to measure the loss of the optical TSVs. Input to an optical TSV is provided from an 830-nm wavelength laser source using a single mode optical fiber. The output power from the optical TSV is measured using a photodetector held on the other end of the optical TSV.

For a large number of the fabricated 390-μm tall and 118-μm diameter SU-8 core optical TSVs (2-μm thick silicon dioxide cladding), the average measured optical loss is 0.59 dB with a standard deviation of 0.15 dB. Fig. 13(b) shows the distribution of the measured optical losses of the fabricated optical TSVs. In addition, the average measured optical loss is found to be the same when the measurements are performed by reversing the wafer demonstrating symmetric losses as expected. Previous work on optical vias measured higher insertion loss for similar sized vias [34], [35]. Losses due to reflection are minimized using an index matching gel between the fiber and the optical TSVs.

IV. Conclusion

Novel polymer-enhanced photo-defined electrical and optical TSVs were demonstrated for silicon interposers. The two novel electrical TSVs presented in this paper were polymer-clad TSVs and polymer-embedded vias. High-frequency measurements and simulations were demonstrated for the fabricated scaled polymer-embedded vias and a comparison with conventional TSV simulations was demonstrated. In addition, resistance measurements were performed for the



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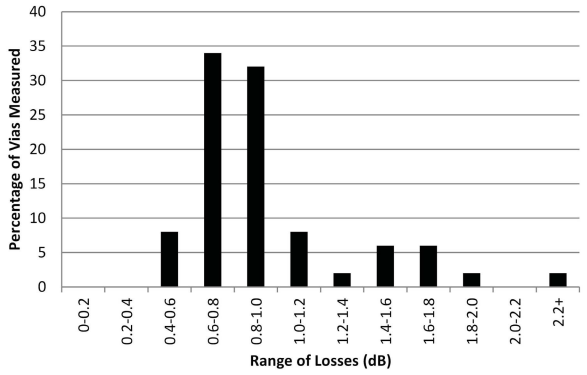

(b)

Fig. 13. Optical loss measurements for the fabricated optical TSVs. (a) Setup to measure optical loss of the fabricated optical TSVs with an inset image showing optical fiber in contact with an optical TSV. (b) Distribution of the measured optical losses.

fabricated electrical TSVs demonstrating high yield, while optical losses were measured for the fabricated optical TSVs demonstrating lower optical losses compared with the prior work for similarly sized optical vias.

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Paragkumar A. Thadesar (S'09) received the B.E. degree in electronics and communication engineering, with a gold medal, from V.V.P. Engineering College, India, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2011, where he is currently pursuing the Ph.D. degree in electrical and computer engineering with a focus on microelectronics.

His current research interests include electrical design, fabrication, and high-frequency characterization of through-silicon vias.

Mr. Thadesar received the first-place Best Student Paper Award in the Poster Session at the IEEE Global Interposer Technology Workshop, in 2012, and the third-place Microelectronics Foundation Prize at the IMAPS International Conference and Exhibition on Device Packaging in 2013.

Muhannad S. Bakir (SM'12) received the B.E.E. degree from Auburn University, Auburn, AL, USA, in 1999, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 2003.

He is currently an Associate Professor and the ON Semiconductor Junior Professor with the School of Electrical and Computer Engineering, Georgia Tech. He is the Editor of *Integrated Interconnect Technologies for 3-D Nanoelectronic Systems* (Artech House, 2009).

Dr. Bakir is a member of the International Technology Roadmap for Semiconductors Technical Working Group for Assembly and Packaging. He was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium, and he received the 2012 DARPA Young Faculty Award. He is a recipient of the 2011 IEEE Components, Packaging and Manufacturing Technology Society Outstanding Young Engineer Award.